



03500.016946.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TACHIO ONO

Application No.: 10/500,803

§ 371(c) Date: July 7, 2004

Intl. Appl. No.: PCT/JP03/00518

Intl. Filing Date: January 22, 2003

For: STORAGE APPARATUS AND
CONTROL METHOD

Examiner: A. Khokhar

Group Art Unit: 2622

February 19, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, Applicant respectfully directs the Examiner's attention to the documents listed below and on the enclosed Form PTO-1449. A copy of each of the documents listed is enclosed.

- (1) Japan 02-294757
- (2) Japan 09-011585

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

February 19, 2008

(Date of Deposit)

Michael J. Guzniczak (Reg. No. 59,820)

(Name of Attorney for Applicant)

Signature

February 19, 2008

Date of Signature

These documents were cited during prosecution of Japan 2002-024609, from which the above-identified application claims priority under 35 U.S.C. § 119. A copy of a Japanese Office Action, mailed January 22, 2008, is enclosed.

English language abstracts for the documents (1) and (2) have been located and are enclosed for the Examiner's consideration.

In addition, Applicant herewith submits a partial translation of the marked portion of the Japanese Office Action, in which the JPO Examiner provides his rationale for refusal as follows:

"In Fig.3 and line 8 of the right-hand lower column of page 7 to line 19 of the left-hand upper column of page 8 of the document 1 and paragraphs [0017] to [0020] of the document 2, it is disclosed that when a plurality of host apparatuses are connected to a peripheral apparatus which includes a plurality of interface circuits, through those interface circuits, the peripheral apparatus so operates that when one of the plurality of interface circuits receives data, other interface circuit is disabled and when such communication is completed, the other interface circuit is enabled. Therefore, it is well known art for a person skilled in the art to effect exclusive control of accesses from the plurality of host apparatuses by disabling the interface of the peripheral apparatus to which the plurality of host apparatuses are connected through the plurality of interface circuits."

"It should be noted that it would have been obvious for a person skilled in the art to use an interface conforming with IEEE1394-1995 standards and extended standards thereof or USB1.1 standards and extended standards thereof."

"In addition, it is not recognized that there is difficulty in applying the above-described well-known art to a storage apparatus and a digital video camera."

The concise explanation of relevance for each of the documents is believed to be satisfied by the enclosed English abstracts and also by the translated portions of the Japanese Office Action. See MPEP § 609.

This Information Disclosure Statement is accompanied by a Request For Continued Examination (RCE) Transmittal. Since the thus-refiled application has not yet received a first Office Action, it is believed that the Information Disclosure Statement is timely. See 37 C.F.R. § 1.97(b)(3). Accordingly, the Examiner is urged to study this information in its entirety and to form an independent determination of the materiality of the information to the claimed invention. Additionally, the Examiner is requested to indicate that this information has been considered by initialling the appropriate portion of the Form PTO-1449 and returning the initialed form to Applicant with the next communication.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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